Product Specification

400Gb/s 50m OSFP SR4 Transceiver module

Product Features

- Up to 106.25 Gbps data rate per channel by PAM4 modulation
- Integrated 850nm VCSEL array and PD array
- 4x106. 25Gb/s electrical interface (400GAUI-4)
- Hot-pluggable
- Compliant to OSFP MSA 5.0
- Compliant with CMIS 4.0
- Maximum power consumption 9W
- Single +3.3V power supply
- Case temperature range: 0 ~ +70℃
- RoHS 2.0 complaint

Applications

- Data centers and Cloud
- Switch & Router Connections

Part No.	Specifications									Application
	Package	Data rate	Laser	Optical Power	Detector	Sensitivity	Temp	Reach	Other	
400G-OSFP-SR4-50M	OSFP	400G	850nm VCSEL	-4.6 ~ 4dBm	PIN	-6.4+TECQ @1.8<TECQ ≦4.4dB	0~70℃	50m	DDM	

Module Block Diagram

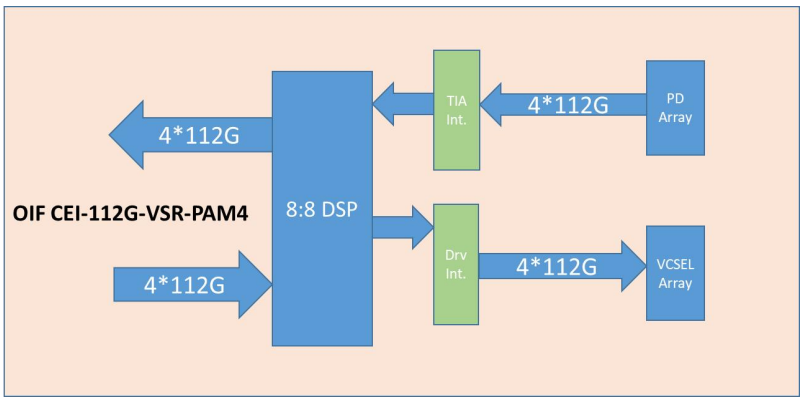

Figure 1. Module Block Diagram

Pin function definitions

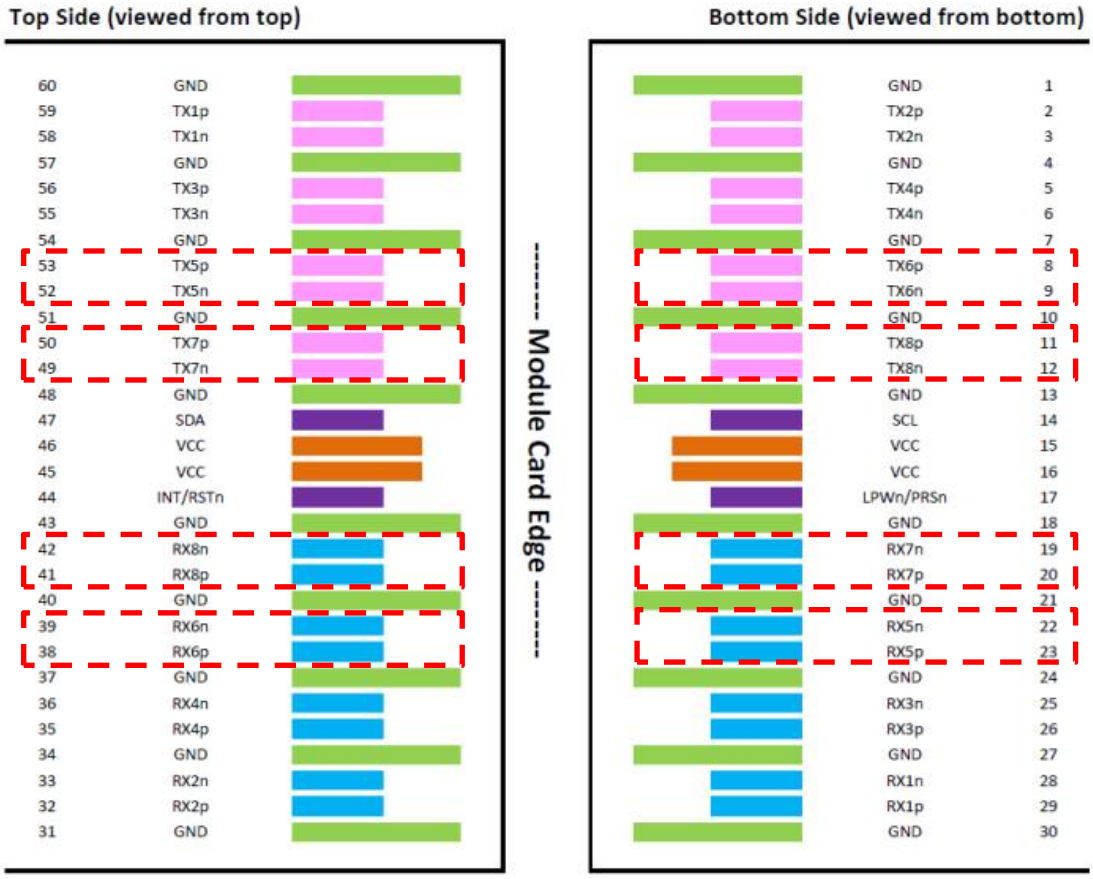

Figure 2. OSFP400 400G contact assignment

Note: For OSFP112 400G SR4 end, Only CH1~CH4 available. CH5~CH8 not connect, TX5~8p/n,RX5~8p/n not connect.

Pin#	Symbol	Description	Logic	Direction	Plug Sequence	Notes
1	GND	Ground			1	
2	TX2p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
3	TX2n	Transmitter Data Inverted	CML-I	Input from Host	3	
4	GND	Ground			1	
5	TX4p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
6	TX4n	Transmitter Data Inverted	CML-I	Input from Host	3	
7	GND	Ground			1	
8	TX6p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
9	TX6n	Transmitter Data Inverted	CML-I	Input from Host	3	
10	GND	Ground			1	
11	TX8p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
12	TX8n	Transmitter Data Inverted	CML-I	Input from Host	3	
13	GND	Ground			1	
14	SCL	2-wire Serial interface clock	LVCMOS-I/O	Bi-directional	3	Open-Drain with pull-up resistor on Host
15	VCC	+3.3V Power		Power from Host	2	
16	VCC	+3.3V Power		Power from Host	2	
17	LPWn/PRSn	Low-Power Mode / Module Present	Multi-Level	Bi-directional	3	See pin description for required circuit
18	GND	Ground			1	
19	RX7n	Receiver Data Inverted	CML-O	Output to Host	3	
20	RX7p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
21	GND	Ground			1	
22	RX5n	Receiver Data Inverted	CML-O	Output to Host	3	
23	RX5p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
24	GND	Ground			1	
25	RX3n	Receiver Data Inverted	CML-O	Output to Host	3	
26	RX3p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
27	GND	Ground			1	
28	RX1n	Receiver Data Inverted	CML-O	Output to Host	3	
29	RX1p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
30	GND	Ground			1	
31	GND	Ground			1	
32	RX2p	Receiver Data Non-Inverted	CML-O	Output to Host	3	

Pin#	Symbol	Description	Logic	Direction	Plug Sequence	Notes
33	RX2n	Receiver Data Inverted	CML-O	Output to Host	3	
34	GND	Ground			1	
35	RX4p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
36	RX4n	Receiver Data Inverted	CML-O	Output to Host	3	
37	GND	Ground			1	
38	RX6p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
39	RX6n	Receiver Data Inverted	CML-O	Output to Host	3	
40	GND	Ground			1	
41	RX8p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
42	RX8n	Receiver Data Inverted	CML-O	Output to Host	3	
43	GND	Ground			1	
44	INT/RSTn	Module Interrupt / Module Reset	Multi-Level	Bi-directional	3	See pin description for required circuit
45	VCC	+3.3V Power		Power from Host	2	
46	VCC	+3.3V Power		Power from Host	2	
47	SDA	2-wire Serial interface data	LVCMOS-I/O	Bi-directional	3	Open-Drain with pull-up resistor on Host
48	GND	Ground			1	
49	TX7n	Transmitter Data Inverted	CML-I	Input from Host	3	
50	TX7p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
51	GND	Ground			1	
52	TX5n	Transmitter Data Inverted	CML-I	Input from Host	3	
53	TX5p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
54	GND	Ground			1	
55	TX3n	Transmitter Data Inverted	CML-I	Input from Host	3	
56	TX3p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
57	GND	Ground			1	
58	TX1n	Transmitter Data Inverted	CML-I	Input from Host	3	
59	TX1p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
60	GND	Ground			1	

Optical Interface

The MPO-12 connectors for OSFP112 400G SR4.

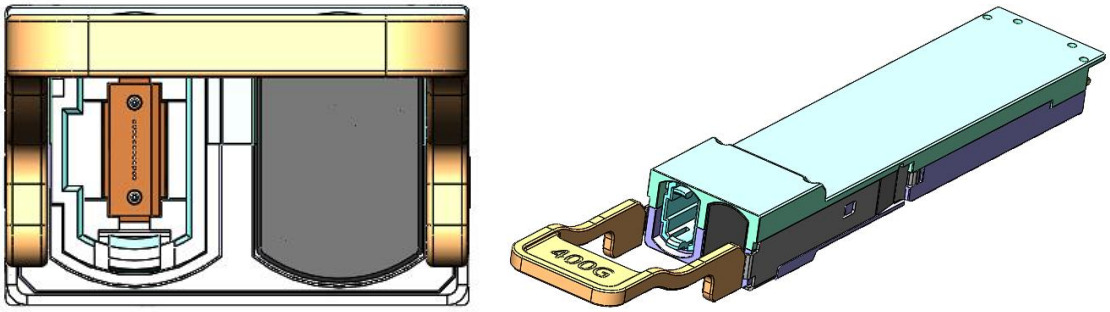

Figure 3. Optical lane assignments

Absolute Maximum Ratings

Parameter	Symbol	Unit	Min	Max
Storage Temperature Range	Ts	°C	-40	85
Relative Humidity	RH	%	5	95
Maximum Supply Voltage	Vcc3	V	-0.5	3.6

Recommended Operating Conditions

Parameter	Symbol	Unit	Min	Typ	Max
Operating Case Temperature Range	Tc	°C	0		70
Power Supply Voltage	Vcc	V	3.14	3.3	3.46
Power Consumption	PDISS	W			9
Pre-FEC Bit Error Ratio	BER				2.4E-4
Link Distance over OM3	L	m			30
Link Distance over OM4	L	m			50

Low Speed Electrical signal

Parameter	Symbol	Min	Max	Unit	Condition
SCL and SDA	VOL	0	0.4	V	IOL(max)=3.0mA for fast mode, 20mA for Fast-mode plus
	VOH	Vcc-0.5	Vcc+0.3	V	
SCL and SDA	VIL	-0.3	Vcc*0.3	V	
	VIH	Vcc*0.7	Vcc +0.5	V	
Capacitance for SCL and SDA I/O pin	Ci		14	pF	
Total bus cpacitive load for SCL and SDA	Cb		100	pF	3.0k Ohms Pull up resistor,max
			200	pF	1.6k Ohms Pull up resistor,max
LPMode/TxDis,Reset and ModeSelL	VIL	-0.3	0.8	V	|Iin| </= 125uA for Vin < Vcc
	VIH	2	Vcc + 0.3	V	
IntL/RxLOS	VOL	0	0.4	V	IOL=2.0mA
	VOH	VCC - 0.5	VCC + 0.3	V	10k ohms pull-up to Host Vcc
ModPrsL	VOL	0	0.4	V	IOL=2.0mA
	VOH			V	ModPrsL can be implemented as a short-circuit to GND on the module

High Speed Electrical signal

Parameter	Min	Typical	Max	Unit	Notes
Receiver electrical output characteristics at TP4					
Signaling rate per lane		53.125		GBd	
AC common-mode output voltage(RMS)		-	17.5	mV	
Differential peak-to-peak output voltage			900	mV	
Near-end ESMW (Eye symmetry mask width)		TBD		UI	
Near-end Eye height, differential	24			mV	
Near-end vertical eye closure			7.5	dB	
Far-end ESMW (Eye symmetry mask width)		TBD		UI	
Far-end Eye height, differential	24			mV	
Far-end vertical eye closure			7.5	dB	
Far-end pre-cursor ISI ratio		TBD		%	
Common mode to differential conversion return loss	802.3ck 120G-1			dB	
Effective return loss	TBD			dB	
Differential termination mismatch			10	%	
Transition time (min, 20% to 80%)		TBD		ps	
DC common mode voltage	-350		2850	mV	
Transmitter electrical input characteristics at TP1					
Signaling rate, per lane		53.125		GBd	
Differential pk-pk input voltage tolerance	900			mV	
Common-mode to differential return loss	802.3ck Equation (120G-1)				
Effective return loss	TBD				
Differential termination mismatch			10	%	
Module stressed input test	See 120G.3.4.1				
Single-ended voltage tolerance range	-0.4		3.3	V	
DC common-mode voltage	-350		2850	mV	

Optical Specifications

Parameter	Min	Typical	Max	Unit	Notes
Transmitter					
Signaling rate each lane	53.125±100ppm			GBd	
Lane Wavelength Range		850		nm	
RMS Spectral width			0.6	nm	
Modulation Format	PAM4				
Average Optical Power per lane	-4.6		4	dBm	

Outer Optical Modulation Amplitude (OMAouter), each lane for TDECQ<=1.8dB for 1.8<TDECQ<=4.4dB	 -2.6 -4.4+TDECQ		 3.5 3.5	dBm	
Outer Optical Modulation Amplitude (OMAouter), each lane for TECQ<=1.8dB for 1.8<TECQ<=4.4dB	 -2.6 -4.4+TECQ		 3.5 3.5	dBm	
Transmitter and Dispersion Eye Closure for PAM 4, each Lane			4.4	dB	
Transmitter Eye Closure for PAM4(TECQ), each Lane			4.4	dB	
Extinction Ratio	2.5			dB	
Transmitter excursion ,each lane			2	dB	
Transmitter transition time,each lane			17	ps	
Average Launch Power per Lane @ TX Off State			-30	dBm	
Relative Intensity Noise12(OMA)			-131	dB/Hz	
Optical Return Loss Tolerance			12	dB	
Encircled Flux	>=86% at 19um <=30% at 4.5um			dB	
Receiver					
Signaling rate each lane	53.125±100ppm			GBd	
Lane Wavelength Range		850		nm	
Modulation Format	PAM4				
Damage Threshold	5			dBm	
Average Receive Power, each lane	-6.4		4	dBm	
Receiver Power, each lane (OMA)			3.5	dBm	
Receiver Sensitivity each lane (OMAouter) for TECQ<=1.8dB for 1.8<TECQ<=4.4dB			 -4.6 -6.4+TECQ	dBm	
Receiver reflectance			-12	dB	
Stressed Receiver Sensitivity (OMAouter), each			-2	dBm	
Stressed Conditions for Stress Receiver Sensitivity					
Stressed Eye Closure for PAM4 (SECQ) ,Lane under Test		4.4		dB	
OMAouter of each Aggressor Lane		3.5		dBm	
RX_LOS_Assert Min/Max	-15.0			dBm	
RX_LOS_De-Assert Min/Max			-8.9	dBm	
RX_LOS_Hysteresis		1.5		dB	

Mechanical Dimensions

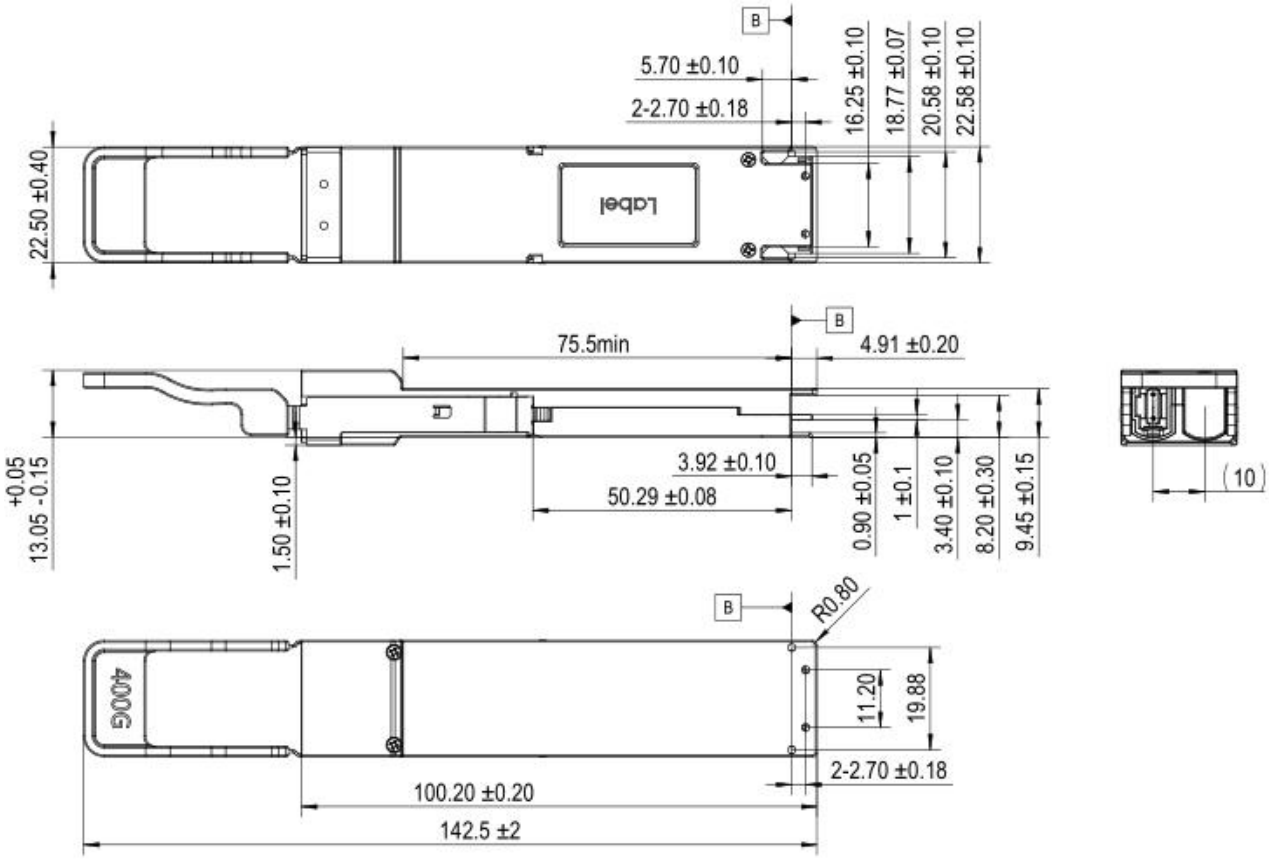

Figure 4. Module Mechanical Dimensions